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BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte CHUL KYU KANG, YONG SUNG PARK,
JIN WOO PARK, and DONG SUN LEE

Appeal 2021-005128
Application 15/979,099
Technology Center 2600

Before CAROLYN D. THOMAS, HUNG H. BUI, and
MICHAEL J. ENGLE, *Administrative Patent Judges*.

ENGLE, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellant[1] appeals under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1–9 and 11–18, which are all of the claims pending in the application. We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

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[1] We use the word "Appellant" to refer to "applicant" as defined in 37 C.F.R. § 1.42(a). Appellant identifies Samsung Display Co., Ltd. as the real party in interest. Appeal Br. 1.

TECHNOLOGY

The application relates to a "circuit stage" for display devices. Spec. ¶¶ 2–7.

ILLUSTRATIVE CLAIM

Claim 1 is illustrative and reproduced below with certain limitations at issue emphasized:

1. A circuit stage comprising:

a first transistor comprising a first electrode and a gate electrode, the first electrode being coupled to a first input terminal, and the gate electrode being coupled to a second input terminal and configured to receive a first clock signal;

an output circuit coupled to the second input terminal and a second power input terminal, and configured to receive the first clock signal such that *the output circuit and the gate electrode of the first transistor are both configured to receive the first clock signal*, and the output circuit is configured to supply a scan signal to an output terminal in accordance with voltages of a first node and a second node;

an input circuit coupled to a second electrode of the first transistor and to a third input terminal, the third input terminal being configured to receive a first control clock signal, the input circuit being configured to control voltages of the second node and a third node;

a first driving circuit coupled to a first power input terminal and to a fourth input terminal configured to receive a second control clock signal, the first driving circuit being configured to control the voltage of the second node; and

a second driving circuit coupled to the fourth input terminal and the third node, and configured to control the voltage of the first node,

wherein the output circuit comprises:

> a ninth transistor coupled between the second input terminal, to receive the first clock signal, and the first node, a gate electrode of the ninth transistor being coupled to the second node; and
>
> a tenth transistor coupled between the second input terminal, to receive the first clock signal, and the output terminal, a gate electrode of the tenth transistor being coupled to the first node.

REFERENCES

The Examiner relies on the following references as prior art:

Name	Number	Date
Chen	US 2017/0004775 A1	Jan. 5, 2017
Jang	US 2014/0055444 A1	Feb. 27, 2014
Murakami	US 2015/0279480 A1	Oct. 1, 2015

REJECTIONS

The Examiner makes the following rejections under 35 U.S.C. § 103:

Claims	References	Final Act.
1–5, 11–14, 18	Jang, Chen	2–9
6–9, 15–17	Jang, Chen, Murakami	10–13

ISSUE

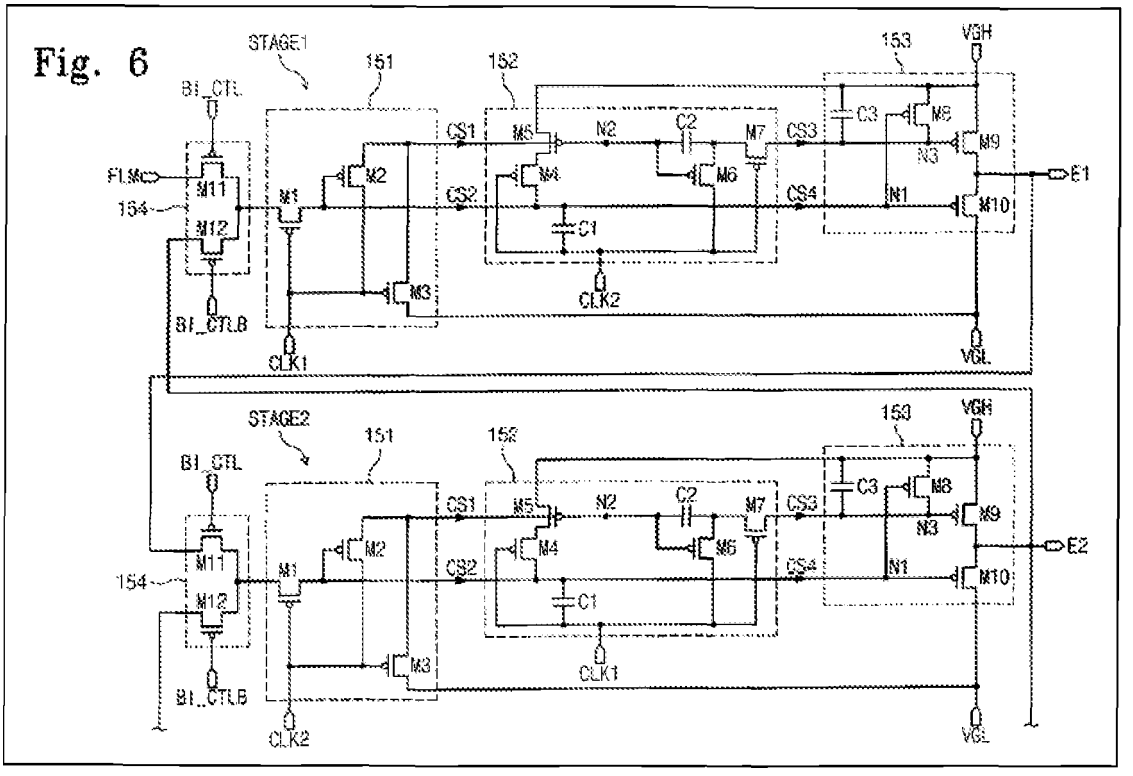
Did the Examiner err in finding the combination of Jang and Chen teaches or suggests "the output circuit and the gate electrode of the first transistor are both configured to receive the first clock signal," as recited in claim 1?

ANALYSIS

Claim 1 recites "the output circuit and the gate electrode of the first transistor are both configured to receive the first clock signal." Thus, the *same* signal must be received by both components and that signal must be a *clock* signal. Independent claim 13 recites a commensurate limitation.

The Examiner relies on Jang for disclosing all limitations of claim 1 except the same clock signal being connected to both the output circuit and the gate electrode of the first transistor, for which the Examiner instead turns to Chen. *See* Final Act. 3–5; Ans. 6.

Figure 6 of Jang is reproduced below:



Jang's Figure 6, as reproduced above, illustrates a "circuit diagram[] of stages of an emission control driver of an organic light emitting display device." Jang ¶ 118. The Examiner maps "M11" (in the upper left of Figure 6) to the claimed "first transistor." Final Act. 3. The signal input to the gate electrode of M11 is labeled "BI_CTL." *Id.*

The Examiner maps "M9-M11 and C3" (in the upper right of Figure 6) to the claimed "output circuit." Final Act. 3. The relevant input to the Examiner's output circuit is labeled "VGH." *Id.*

BI_CTL and VGH are not the *same* signal, which is why the Examiner relies on Chen. Figure 4 of Chen is reproduced below:

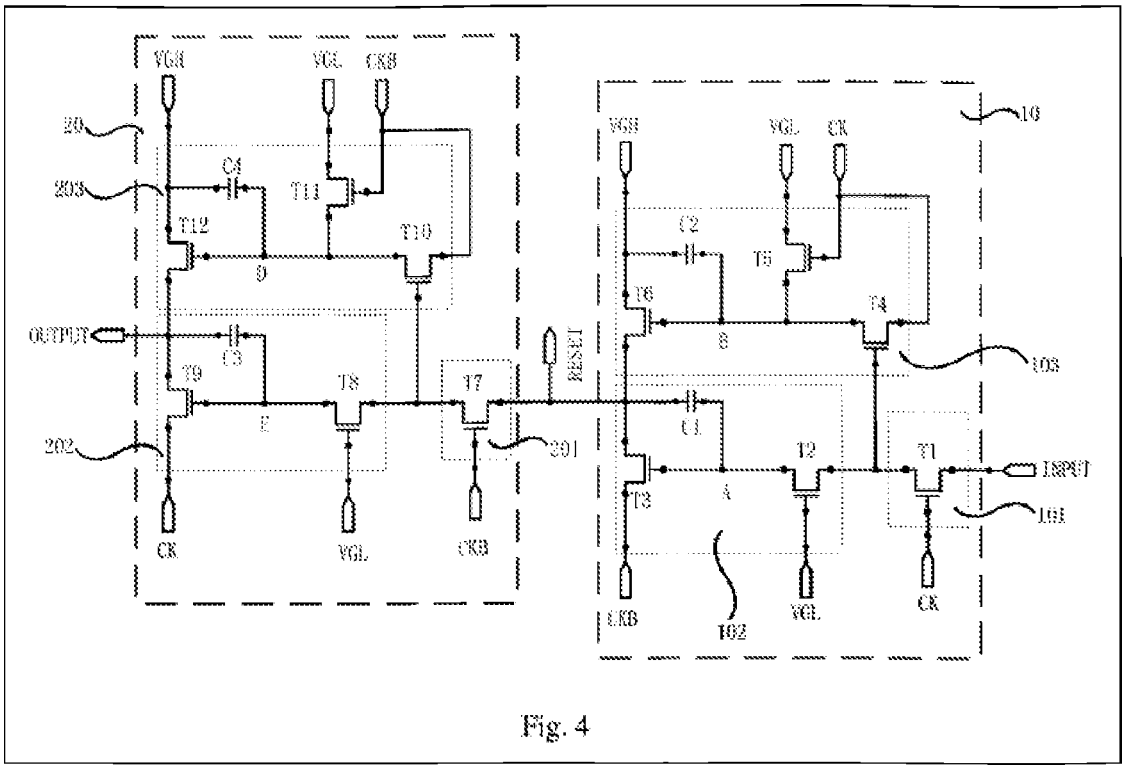


Fig. 4

Chen's Figure 4, as reproduced above, "is a schematic diagram of detailed structure of the shift register unit" of Chen's invention. Chen ¶ 27. The "Examiner is using Chen for the synchronization of first transistor and output unit since Jang teaches all the limitations of the claims with the exception of a clock connection of input transistor and output unit." Ans. 6. In particular, the Examiner relies on the clock signal CK as being provided to both the input transistor (T1, in the lower right of Figure 4) and the output circuit (including at least T9, in the lower left of Figure 4). *Id.* at 5–6.

The Examiner determines:

> [I]t would have been obvious . . . to provide a clock signal connected to the output circuit and to the gate of the first transistor as taught by Chen with the benefit that clock signal should provide an output signal from the shift register when T9

> is ON as shown in figure 7 while an input or start signal is provided to the shift register when T1 is ON as also shown in figure 7. In other words, CK should provide synchronization for the output circuit and the first transistor as shown in figures 5-8.

Final Act. 5.

Elsewhere, however, the Examiner also states that in Jang, "BI_CTL is considered a clocked signal" because "BI_CTL comprises high level and low level for different periods . . . with intervals . . . since BI_CTL is high during a particular time and low during other particular time." Ans. 3. According to the Examiner, claim 1 "does not recite 'regular intervals' or 'constant intervals'" are required for a clock signal and "thus it can be irregular." *Id.* at 3–4.

Appellant argues that it is not clear whether the Examiner's combination is (A) replacing Jang's VGH with its BI_CTL or (B) replacing both VGH and BI_CTL of Jang with Chen's CK. *See, e.g.*, Appeal Br. 12. Either way, we agree with Appellant that the Examiner has not shown a person having ordinary skill in the art would have had reason to make the Examiner's proposed change. *See id.* at 12–16.

In Jang, VGH is simply a high voltage signal. *See* Jang ¶¶ 90 ("Hereinafter, *a high level of each signal is referred to as a first level* and a low level, lower than the high level, of each signal is referred to as a second level. In addition, the first voltage VGL has the second level and *the second voltage VGH has the first level*." (emphasis added)), 44 ("The emission control driver 150 is applied with a first voltage VGL and a second voltage VGH having a voltage level higher than that of the first voltage level VGL.").

BI_CTL is described as "a first direction control signal." Jang ¶ 120. "The first direction control signal BI_CTL and the second direction control signal BI_CTLB have different levels from each other." *Id.* ¶ 128. "For instance, when the first direction control signal BI_CTL has a first level (or a high level), the second direction control signal BI_CTLB has a second level (or a low level) lower than the first level." *Id.* "Although not shown in [the timing diagram of] FIG. 9, the first direction control signal BI_CTL has the second level [i.e., low level] . . . ." *Id.* ¶ 144.

Thus, Jang discloses that BI_CTL can be at the "second level" when VGH is at the "first level." Merely replacing VGH with BI_CTL therefore would result in the wrong level for the signal at least some of the time. Similarly, Chen's CK is a clock signal that regularly alternates between high and low, as shown in Figure 3 of Chen, so replacing both VGH and BI_CTL with Chen's CK signal would result in the wrong level for at least one signal some of the time. *See* Appeal Br. 14–16. Even if a person of ordinary skill in the art *could* modify Jang's circuit so that its input transistor's gate electrode and output circuit received the same signal (whether Jang's BI_CTL or Chen's CK), the Examiner has not explained sufficiently why a person of ordinary skill *would* do so. *See, e.g.*, *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) ("[O]bviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention."). As the Supreme Court has said, "a patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). Here,

the Examiner says that Chen's "CK should provide synchronization for the output circuit and the first transistor," but fails to address sufficiently whether or why a person of ordinary skill would have wanted that or otherwise known to make the change. Final Act. 5.

Accordingly, we do not sustain the Examiner's rejections of claims 1–9 and 11–18.

OUTCOME

The following table summarizes the outcome of each rejection:

Claim(s) Rejected	35 U.S.C. §	Reference(s)/Basis	Affirmed	Reversed
1–5, 11–14, 18	103	Jang, Chen		1–5, 11–14, 18
6–9, 15–17	103	Jang, Chen, Murakami		6–9, 15–17
Overall Outcome				1–9, 11–18

REVERSED